REMARKS

Applicants' representative believes that claims 1-29 are pending in the current application, although, for reasons discussed below, the office action dated December 8, 2006 ("Office Action") appears to introduce a certain ambiguity as to which claims are currently pending. In the Office Action, the Examiner apparently maintained a restriction of claims 30-43 from claims 1-29, based on a lengthy justification, objected to claims 10 and 14, rejected claims 9-29 under 35 U.S.C. § 112, second paragraph, as being indefinite, appears to have rejected claim 9 under 35 U.S.C. § 102(b) as being anticipated by Fukuzawa et al., U.S. Patent No. 6,089,129 ("Fukuzawa"), rejected claims 10-12, 14, and 28-29 under 35 U.S.C. § 103(a) as being unpatentable over Fukuzawa, provisionally rejected claim 9 under the judicially created doctrine of nonstatutory double patenting, and conditionally allowed claims 13 and 15-27. Applicants' representative respectfully traverses the 35 U.S.C. § 102(b) and U.S.C. § 103(a) rejections based on Fukuzawa.

Restriction Requirement

First, Applicants' representative respectfully points out that the lengthy justification for maintaining the restriction requirement appears to be inconsistent. Initially, Group I is correctly identified as including claims 1-19, in section 1 of the Office Action. However, at the bottom of page 2 of the Office Action, and throughout the rest of the length justification, Group I appears to be misidentified as claims 9-29. Moreover, claims 1-8 are not mentioned in the remainder of the Office Action, and are neither rejected nor allowed. Applicants' representative does not understand exactly which claims the Examiner considers to be currently pending, and respectfully requests a clarification. Applicants' representative believes that claims 1-29 ought to be currently pending.

Applicants' representative believes that the Examiner's justification for maintaining the restriction requirement is unfounded. Claims 30-43, as previously pointed out by Applicants' representative, includes much language that is nearly identical to language contained in claims 16, 18, 20-22, and 25-27. The Examiner's statement, in

section 7 of the Office Action, that these claims depend from claim 9 rather than claim 1 is quite beside the point. The point is that Group II overlaps almost entirely with Group I, and there is no justification for restricting claims that will require an almost identical, redundant searching effort. The Examiner's statement, in section 6 of the Office Action, also makes little sense. The details of the routing logic recited in Group II claims, i.e. claims 30-43, are also included, often using identical language, in Group I claims. The dependency of the various claims is immaterial. The fact is, a search for the subject matter to which claims 1-29 are directed necessarily requires a search for the subject matter of claims 30-43. The overlap would seem to be too great to be dismissed by an ambiguous reference to claim details. In section 5 of the Office Action, the Examiner states that "a router may be used for load balancing, mirroring in other storage-shelf systems." Applicants' representative cannot find a single occurrence of the word "mirroring" or the phrase "load balancing" in the current application. There is absolutely no justification in the current application for this statement, and the Examiner has not yet cited a reference directed to a storage-shelf router of any kind. Thus, the Examiner would seem not to have identified any basis for this statement. Furthermore, the Examiner's statement that "claim 30 does not include any recitation of the ability of a path-controller to accept data and commands from either a first storage-shelf-router integrated circuit or a last storage-shelf-router integrated circuit" makes no sense. Claim 30 is directed to routing logic within a local storage-shelf router, and not to path-controllers within path-controller cards. The Examiner's statement, in section 3 of the Office Action, that "claims 1,9 do not have overlapping subject matter with claim 30 9as isindicated above)" is completely incorrect. As pointed out in the original traversal, claim 30 is directed to a "routing logic component within a local storage-shelf router,: while claim 1 is directed to a "storage-shelf router that contains first and second storage-shelf-router integrated circuits," each of which includes "routing logic." There is logical overlap between claims 1 and 30, as explicitly stated in the claims. Finally, the Examiner spends a great deal of time comparing claim 30 to claim 1, but, in fact, these comparisons are irrelevant. What is relevant is that claims 30-43 are directed to a routing-logic component of the storage-shelf router of claims 1 and 9, and most of the details of routing

logic recited in claims 30-39 are also recited in claims 1-29. The proper comparison is between groups of claims, rather than individual claims.

For all of these reasons, the Examiner's restriction of claims 1-29 from claims 30-43 is unfounded and incorrect, and Applicants' representative respectfully requests that the Examiner reconsider the restriction requirement. Applicants' representative also requests that, in reconsidering the restriction requirement, the Examiner please correct the ambiguity with respect to claims 1-8.

Claim Objections

Applicant's representative has amended claim 10 to address the Examiner's first two claim objections, and wishes to than the Examiner for pointing out these errors. With regard to the objection to claim 14, Applicant's representative believes that claim 14 is correct, as originally written. Claim 14 reads:

> 14. The storage-shelf-router integrated circuit of claim 9 wherein the *storage-shelf-router integrated circuit* **is assigned** a unique number and **is linked** through the first communications-medium port and a first communications medium to a first entity and **is linked** through the second communications-medium port and a second communications medium to a second entity, the first entity one of
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> a remote device external to the storage shelf, and
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> a storage-shelf-router integrated circuit having a unique number less than the assigned unique number, and
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> the second entity one of
>
> a remote device external to the storage shelf, and
>
> a storage-shelf-router integrated circuit having a unique number greater than the assigned unique number. (emphasis added)

In claim 14, as shown above with emphasis, the phrase "storage-shelf-router integrated circuit is the subject of the sentence, and the sentence contains three verbal phrases, shown in bold. The phrase ", the first entity one of ..." is a clause that modifies the independent clause. Introduction os the word "is" into this clause, as suggested by the Examiner, would be improper, and would transform the dependent clause into an independent clause, only one of which can be included in a proper English-language sentence.

35 U.S.C. § 112, second paragraph, Rejections

Applicants' representative has amended claims 9, 12, and 13 to address certain of the Examiner's 35 U.S.C. § 112, second paragraph rejections, and again wishes to thank the Examiner for pointing out these errors. However, the rejection of claim for lack of antecedent basis is incorrect. Claim 10 reads:

> 10. (currently amended) The storage-shelf-router integrated circuit of claim 9 wherein **each** of the two communications-medium ports includes a first-in-first-out buffer into which commands and data received by the communications-medium port are written, and from which commands and data received by the communications-medium port are accessed by the routing logic. (emphasis added)

The subject of the clause beginning with the word "wherein" is "each," as shown in bold, above. The antecedent for the phrase "the communications-medium port" is the phrase "each of the two communications-medium ports," in both occurrences of the phrase.

35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) Rejections

It is unclear from the Office Action whether the Examiner has rejected claim 9 under 35 U.S.C. § 102(b) or under 35 U.S.C. § 103. Applicants' representative assumes that the Examiner's statement, in section 16 of the Office Action, includes a typographical error, and that claim 9 is rejected under 35 U.S.C. § 102(b). Regardless, Fukuzawa is unsuitable as a reference either for an anticipation rejection or for an obviousness-type rejection.

Fukuzawa does not disclose a storage shelf, storage-shelf router, or single-integrated-circuit implementation of a storage shelf router. The Examiner apparently has selected a disclosed component of a large, main-frame computer from Figure 1 of Fukuzawa as representing a storage shelf, perhaps because the component includes disk drives. However, Fukuzawa does not one teach, mention, or suggest that this component is a storage shelf, instead explicitly, and in numerous passages, correctly identifying the component as an I/O subsystem of a mainframe computer (*see*, *e.g.*, the label "I/O

Subsystem" in Figure 1 of Fukuzawa and column 6, lines 4-5). Fukuzawa is concerned with a method for backing up data from a personal computer or workstation, referred to as an "open system" by Fukuzawa, as shown as system B 110 in Figure 1, to a mainframe computer (100 in Figure 1), as explained in Fukuzawa's Summary of the Invention starting on line 65 of column 1.

First, as has been discussed at length in previously filed responses, claim 9 is directed to a storage-shelf-router integrated circuit. The phrase "integrated circuit" has a very well-defined meaning in electronics and computing - namely an electronic circuit, generally quite complex, manufactured within one or more thin layers above a single silicon substrate. An integrated circuit is also referred to as a "chip." The current application clearly states, in many places, that the current application is directed to a single-integrated-circuit implementation of a storage-shelf router, as, for example, in the following passage of the Summary of the Invention section:

> In one embodiment, each storage-shelf router is an integrated circuit that includes processing elements, multiple memories, a layered logic architecture, two complete FC ports for interconnecting the storage-shelf router to high-bandwidth communications media, and a number of SATA ports that each provides an interface to an SATA disk.

Much of the current application is devoted to disclosing the architecture of the claimed single-integrated-circuit implementation of the storage-shelf router, including Figures 15-23 and the text, beginning on line 11 of page 40, which refers to these figures.

The Examiner points to Fukuzawa's mainframe-computer disk controller (104) in Figure 1 as teaching a storage-shelf-router integrated circuit. Fukuzawa describes the disk controller as follows, beginning on line 63 of column 6:

> FIG. 3 is a diagram showing a configuration of the disk controller A 104.
> The disk controller A 104 includes a MPU 302 for executing a control system process 307 of the disk controller, a memory 301, a host data transfer dervice 303, a disk/cache device 304, an inter-I/O subsystem data transfer device 305, a data transfer device 306 and a control bus 308 for connecting these devices.

Fukuzawa does not teach. mention, or even vaguely suggest that the disk controller is an integrated circuit. In fact, it clearly is not an integrated circuit, as is manifestly clear from the above-quoted passage. Fukuzawa describes all of the subcomponents of the disk

controller as "devices," and the devices are explicitly stated to be interconnected by a control bus. A control bus is defined, by the on-line Wikipedia encyclopedia, as follows:

> A **control bus** is (part of) a computer bus, used by CPUs for communicating with other devices within the computer. While the address bus carries the information on which device the CPU is communicating with and the data bus carries the actual data being processed, the control bus carries commands from the CPU and returns status signals from the devices, for example if the data is being read or written to the device the appropriate line (read or write) will be active (logic zero).

Control buses are not included in integrated circuits, but are instead used to interconnect integrated-circuit CPUs with other devices, such as I/O subsystem controllers, as is well-known to those familiar with computer hardware, computer architecture, and electrical engineering. More detailed description of control buses can be found in any of numerous computer architecture and computer hardware texts, including "Computer organization and Design," Hennesey and Patterson, Morgan Kaufman Publishers, Inc. 1998, pp. 655-673.

As been discussed at length in previous responses, until the present invention, no one had managed to implement a storage-shelf router as an integrated circuit. It was only with a huge research and design effort that the single-integrated-circuit storage-shelf router that represents on embodiment of the present invention was produced. Applicants' have fairly claimed a storage-shelf-router integrated circuit, having been the first, and only group of inventors, to date, to have successfully designed and implemented a single-integrated-circuit implementation of a storage-shelf router. A large, printed-circuit-board implementation of a mainframe I/O subsystem controller is completely unrelated to a storage-shelf router, particularly a single-integrated-circuit storage-shelf router, and is not a suitable reference for either an anticipation or obviousness-type rejection. The phrase "integrated circuit" is a claim limitation in both independent claims 1 and 29 and has a very well-known meaning in electronics. The Examiner cannot simply ignore such a claim limitation in attempting to read the current claims onto an unrelated device. Current case law and the MPEP clearly state that, to anticipate or make obvious a claim, a cited reference must teach or disclose each and

every claim limitation. Because Fukuzawa does not teach, mention, or suggest an integrated-circuit implementation of a storage-shelf router, let alone any implementation of a storage-shelf router, Fukuzawa cannot possibly anticipate or make obvious the current claims.

As discussed in the current application, in the Summary of the Invention section:

> In one embodiment, each storage-shelf router is an integrated circuit that includes processing elements, multiple memories, a layered logic architecture, two complete FC ports for interconnecting the storage-shelf router to high-bandwidth communications media, and a number of SATA ports that each provides an interface to an SATA disk. FC ports link all storage-shelf routers within the storage shelf together to an internal fabric space within the storage-shelf router. The interconnected storage-shelf routers are linked to two separate, partially external fabric spaces, such as partially external FC arbitrated loops, that interconnect the storage shelf with a disk-array controller or other controlling component.
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> A set of interconnected storage-shelf routers within a storage shelf, can be accessed through a single port of an FC arbitrated loop or other high-bandwidth communications medium. In other words, each storage shelf can represent a single node of an FC arbitrated loop, rather than a set of nodes equal to the number of disk drives within the storage shelf, as in many current disk arrays. Therefore, interconnection of disk drives in the storage shelf by storage-shelf routers essentially eliminates the cumulative node delay problem inherent in current storage shelves in which each disk drive is directly connected to one or more FC arbitrated loops. Because, in one implementation, 8 storage-shelf routers can be interconnected within a storage shelf to provide highly available interconnection of 64 disk drives within the storage shelf to an FC arbitrated loop via a single FC-arbitrated-loop port, a single FC arbitrated loop including a disk-array controller may interconnect as many as 8,000 individual disk drives to the disk-array controller within a disk array with sufficient interconnection redundancy to allow for highly available operation. When high availability is not needed, 8 storage-shelf routers can provide interconnection of 125 disk drives within a storage shelf, in turn providing for interconnection of as many as 16,000 individual disk drives via a single FC arbitrated loop including a disk-array controller. Thus, instead of employing a single FC arbitrated loop, or pair of FC arbitrated loops, for every 125 disk drives within a disk array, the storage-shelf router that represents one embodiment of the present invention may be used to interconnect 8,000 individual disk drives, in a highly available fashion, or 16,000 individual disk drives, without redundant connections, via one, or a pair of, FC arbitrated loops.

Thus a storage-shelf router provides an abstraction to a disk-array controller, allowing the

disk-array controller to access a large number of individual disk drives through a single FC-port address. By contrast, Fukuzawa's I/O subsystem controller requires a host computer, such as the mainframe computer (100 in Figure 1 of Fukuzawa) or PC (110 in Figure 1 of Fukuzawa) to individually address the disks controlled by a disk controller, as discussed beginning on line 27 of column 7 in Fukuzawa. An I/O subsystem controller is not a storage shelf, as is well known to those familiar with computer architectures, disk arrays, and computer hardware systems. The term "storage shelf" is not an arbitrary phrase selected by Applicants, but is a well-known term in the art that describes storage shelves, which are described in great detail in the current application. The Examiner cannot simply rename the dissimilar I/O subsystem controller of Fukuzawa a "storage-shelf router" in order to craft a rejection, just as an Examiner could not rename a CD drive a "magnetic disk drive" in order to read a claim directed to a CD-drive optical storage device onto the disclosure of a magnetic disk drive. Claim terms have the meaning assigned to them in the disclosure, if such definitions are present, or the meaning that one skilled in the relevant art would assign to them. Otherwise, claims would have no chance of providing a definitive scope of a claimed invention, which is their purpose.

Allowable Claims

Applicants' representative wishes to thank the Examiner for the conditional allowance of claims 13 and 15-27. However, Applicants' represent wishes to defer rewriting any claims until the above traversal of the Examiner's 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) rejections is considered. In addition, Applicants' representative respectfully requests that the Examiner clarify the status of claims 1-8, which appear to be neither rejected nor allowed in the Office Action.

In Applicant's representative's opinion, all the claims remaining in the current application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

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